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EXAMINER	
VICARY, KEITH E	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/073,948	RHOADES ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-13,16,17,19-22,32,34,35,38,40,41,44,46,47,50,52,53,56 and 59-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-4,6-9,11-13,16,17,19-22,32,34,35,38,40,41,44,46,47,50,52,53,56 and 59-64.

DETAILED ACTION

1. Claims 1-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 are pending in this office action and presented for examination.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

3. Applicant's arguments made during an interview on 9/8/2008 regarding the pending final rejection made by a previous examiner were persuasive; thus, the current non-final rejection using significantly different prior art references is being issued.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claims 11, 34, 40, 46, and 52 are objected to because the claims do not refer back to another claim as mandated by 37 CFR 1.75(c), as they are all dependent on claim 60.

6. Claims 17, 20, and 60 are objected to because of the following informalities. Appropriate correction is required.

a. Claim 60 recites the limitation "input output system" in line 2, which should presumably be "input/output system" to align with the language of claim 11.

b. Claim 17 recites the limitation "data I/O"; this acronym should be explicitly expanded upon similar to claim 2.

c. Claim 20 recites the limitation "SIMD"; this acronym should be explicitly expanded upon similar to claim 2.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 1 recites both "data packet" and "whole data packet" as limitations; it is indefinite as to whether these two limitations refer to different things, as the specification and the context of the claim imply that a data packet is a "whole" data packet.

d. Claims 2-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 are rejected for failing to alleviate the rejection of claim 1 above.

10. Claim 3 recites the limitation "it" in the third line; that which "it" refers to should be explicitly recited.

11. Claim 7 recites the limitation "the processing elements are operable to control the input device." However, it is indefinite as to what this limitation is trying to convey, as examiner has perused the instant specification and it appears that it is not the processing elements which control the input device, but the thread sequence controller. See, for example, page 33, which discloses "[a] single hardware multi-threaded Thread Sequence Controller manages the issuing of instructions to the P/E array and the I/O engines" wherein the TSC is separate from the processing elements in Figure 4. As another example, see page 52, which discloses that a packet loading thread performs the scheduling of the transfer of packet data from the Distributor into the local memory of the PEs in the processor.

e. Claim 8 is rejected for failing to alleviate the rejection of claim 7 above.

12. Claim 9 recites the limitation "the processing elements are operable to control an output device." However, it is indefinite as to what this limitation is trying to convey, as examiner has perused the instant specification and it appears that it is not the processing elements which control the output device, but the thread sequence controller. See, for example, page 33, which discloses "[a] single hardware multi-threaded Thread Sequence Controller manages the issuing of instructions to the P/E array and the I/O engines" wherein the TSC is separate from the processing elements in Figure 4. As another example, see page 52, which discloses that a packet unloading

thread schedules the transfer of packet data from the local memory of PEs in the processor to the Collector.

13. Claim 34, 40, 46, and 52 recite the limitation "an architecture as claimed in claim 60"; however, it is specifically a "data processing architecture" which is claimed in claim 60.

14. Claim 52 recites the limitation "an architecture or system as claimed in claim 60." It is indefinite as to whether the aforementioned system is referring to the input output system of claim 60, or another system. In the latter case, there is insufficient antecedent basis for a system as claimed in claim 60. In the former case, it is indefinite as to what this system is.

15. Claims 41, 47, and 53 recite the limitation "an architecture as claimed in claim 12"; however, it is specifically a "data processing architecture" which is claimed in claim 12.

16. Claim 53 recites the limitation "an architecture or system as claimed in claim 12." There is insufficient antecedent basis for a system as claimed in claim 12, and it is indefinite as to what this system is.

17. Claims 38, 44, 50, and 56 recite the limitation "an architecture as claimed in claim 17"; however, it is specifically a "data processing architecture" which is claimed in claim 17.

18. Claim 56 recites the limitation "an architecture or system as claimed in claim 17." There is insufficient antecedent basis for a system as claimed in claim 17, and it is indefinite as to what this system is.

19. Claim 32 recites the limitation "an architecture as claimed in claim 1"; however, it is specifically a "data processing architecture" which is claimed in claim 1.

20. Claim 32 recites the limitation "an architecture or system as claimed in claim 1." There is insufficient antecedent basis for a system as claimed in claim 1, and it is indefinite as to what this system is.

21. Claims 63 and 64 recite the limitation "the amount of required processing" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

22. Claims 63-64 recite the limitation "the bandwidth" in line 2. There is insufficient antecedent basis for this limitation in the claim; note that there can be varying bandwidth metrics for various components of an overall data processing architecture.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 1-4, 6-9, 11, 16-17, 20-21, 32, 40, 44, 52, 56, 59-60, and 63-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marsan et al. (Marsan)

(Router Architectures Exploiting Input-Queued, Cell-Based Switching Fabrics in view of Clauberg (WO 97/29613)

25. Consider claim 1, Marsan discloses an input device for receiving an incoming stream of data packets of unpredictable size (page 2, first indented paragraph, input IP datagrams are internally segmented into ATM-like cells); to process data received thereby (page 2, first indented paragraph, internally operates on fixed-size data units called cells);

However, Marsan does not disclose of the manner in which the cells are operated on, and thus does not disclose that a plurality of processing elements processes the data, and the input device is operable to distribute whole data packets of unpredictable size across one or more of said processing elements such that the number of said processing elements across which each whole data packet is distributed is dynamically determined based at least in part on the size of the whole data packet, a data packet greater than a predetermined size being divided into portions and each portion distributed to a respective processing element; and a data packet less than a predetermined size being distributed to a single processing element; wherein the data processing architecture is operable to process at least one data packet at a time.

On the other hand, Clauberg discloses that a plurality of processing elements processes the data (Figure 1, for example; incoming data is processed by 14.1 to 14.5 and 15.1 to 15.5) and the input device is operable to distribute cells across one or more of said processing elements wherein the data processing architecture is operable to process at least one data packet at a time (Figure 1 as above; incoming cells are

processed in parallel and simultaneously within a processing path; demux 12 serves as the distributor of cells).

Clauberg's teaching results in very fast on-the-fly processing of fixed length cells even at very high data transmission rates (Clauberg, page 2, line 31 through page 3, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Clauberg with the invention Marsan in order to achieve very fast on-the-fly processing of fixed length cells even at very high data transmission rates. Note that Clauberg's teaching wherein cells are processed in parallel, when applied to the invention of Marsan wherein packets are divided into cells prior to processing, teach the overall limitations wherein whole data packets of unpredictable size are distributed among one or more of said processing elements such that the number of said processing elements across which each whole data packet is distributed is dynamically determined based at least in part on the size of the whole data packet, a data packet greater than a predetermined size being divided into portions and each portion distributed to a respective processing element; and a data packet less than a predetermined size being distributed to a single processing element (the size of a variable length packet determines how many fixed length cells it is broken up into, and the cells are distributed to the processing elements regardless of packet considerations).

26. Consider claim 2, Clauberg discloses the processing elements are arranged in a single instruction multiple data (SIMD) array (see Figure 1 for example, many processing elements performing the same operation on different data).

27. Consider claim 3, Marsan as modified by Clauberg discloses a whole data packet is allocated to as many processing elements as are necessary to store it and to process it (see the combination of the independent claim; the size of a variable length packet determines how many fixed length cells it is broken up into, and the cells are distributed to the processing elements regardless of packet considerations).

28. Consider claim 4, Marsan and Clauberg discloses the portions are of a fixed size (Marsan, page 2, first indented paragraph, fixed-size data units called cells; Clauberg, page 5, line 16 for example, fixed length cells).

29. Consider claim 6, Marsan as modified by Clauberg discloses the input device is operable to transfer data packets to the processing elements such that not all processing elements receive data (see the combination of the independent claim; the size of a variable length packet determines how many fixed length cells it is broken up into, and the cells are distributed to the processing elements regardless of packet considerations; a smaller packet would not be broken up into enough fixed length cells to send cells to all processing elements).

30. Consider claim 7, Marsan or Clauberg discloses the processing elements are operable to control the input device (an input device can be thought to collectively include the processing elements. Alternatively, Clauberg discloses of using a counter in page 10, line 7, which may be considered as part of the processing elements).

31. Consider claim 8, Marsan or Clauberg discloses the processing elements are operable to control the input device by means of software (it would have been obvious to one of ordinary skill in the art at the time of the invention that software can perform a function of hardware with more flexibility).

32. Consider claim 9, Marsan or Clauberg discloses the processing elements are operable to control an output device (an output device can be thought to collectively include the processing elements. Alternatively, Clauberg discloses from page 9, line 31 to page 10, line 3, of using a clock signal and an output of the processing element to control the mux).

33. Consider claim 59, Marsan or Clauberg discloses said output device is operable to collect processor data packets from the processing elements and to construct an outgoing data packet stream from collected processor data packets (Marsan, page 2, first indented paragraph, cells that are transferred to output interfaces, where they are reassembled into variable-size IP datagrams; Clauberg, Figure 1, Mux 17 constructing output data stream 19).

34. Consider claim 60, Marson or Clauberg discloses said input device and said output device are part of an input output system operable to transmit data to, and receive data from, the processing elements (each reference's input and output device can be collectively considered an input output system, which both transmits data to and receives data from the processing elements).

35. Consider claim 11, Clauberg discloses a plurality of such input/output systems, adapted to support multiple input/output operations (Figure 1, each input or output to and from a specific processing element can be considered a separate input/output system).

36. Consider claim 40, Clauberg discloses the architecture is implemented on a single integrated circuit (page 10, line 18, chip).

37. Consider claim 52, Marson discloses a processor comprising an architecture or system (page 2, first indented paragraph, the overall router is a processor as it processes data).

38. Consider claim 16, Clauberg discloses a first plurality of parallel arrays of processing elements, and second plurality of hardware accelerator units (see Figure 1, processing elements 14.x and 15.x; these can also be considered hardware accelerator

units, although Figure 4B also discloses of a processor and an AAL5 Segmentation and Reassembly unit which also serve as hardware accelerator units).

39. Consider claim 17, Clauberg discloses a plurality of parallel arrays of said processing elements, and a data I/O structure which is operable to transfer data to and from the arrays of processing elements in turn (see Figure 1, processing elements 14.x and 15.x; these can also be considered hardware accelerator units; the IO structure includes the arrows to and from the processing elements).

40. Consider claim 44, Clauberg discloses the architecture is implemented on a single integrated circuit (page 10, line 18, chip).

41. Consider claim 56, Marson discloses a processor comprising an architecture or system (page 2, first indented paragraph, the overall router is a processor as it processes data).

42. Consider claim 20, Marson as modified by Clauberg discloses of a plurality of functional blocks chosen from: a SIMD processing element array, a data input device, a data output device, a hardware accelerator, a data packet buffer and a bus structure for connecting the functional blocks to one another (see Figure 1 and the rejection of the independent claim).

43. Consider claim 21, Clauberg discloses the architecture is implemented on a single integrated circuit (page 10, line 18, chip).

44. Consider claim 32, Marson discloses a processor comprising an architecture or system (page 2, first indented paragraph, the overall router is a processor as it processes data).

45. Consider claim 63, Marsan as modified by Clauberg discloses that the number of processing elements is determined based on the bandwidth and the amount of require processing (it would have been obvious to one of ordinary skill in the art at the time of the invention that additional processing elements are added in order to increase processing capability; note, page 10, line 6, for example, which uses a variable to indicate the number of parallel paths).

46. Consider claim 64, Marsan as modified by Clauberg discloses wherein the size of the packet portions is determined based on the bandwidth and the amount of required processing (it would have been obvious to one of ordinary skill in the art at the time of the invention that the size of the packet portions has a direct correlation with the bandwidth of the router).

47. Claims 12-13, 19, 34-35, 38, 41, 53, and 61-62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marsan and Clauberg as applied to claims 1, 2, 17, and 60 above, and further in view of Kejriwal et al. (Kejriwal) (US 6704794).

48. Consider claims 19, 34 and 38, Marsan and Clauberg do not explicitly disclose each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

On the other hand, Kejriwal discloses of a processing element which is operable to process data stored by that element in accordance with processing steps determined by the data concerned (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

Kejriwal's teaching of detecting whether a cell has packet header information, and only performing packet header operations if there is, enables the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kejriwal with the invention of Marsan and Clauberg in order to enable the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

49. Consider claim 12, Marsan and Clauberg do not explicitly disclose at least one processing element is operable to enter a standby mode of operation in dependence upon data received by that processing element.

On the other hand, Kejriwal discloses of a processing element which is operable to enter a standby mode of operation in dependence upon data received by that processing element (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

Kejriwal's teaching of detecting whether a cell has packet header information, and only performing packet header operations if there is, enables the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kejriwal with the invention of Marsan and Clauberg in order to enable the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

50. Consider claim 13, Clauberg discloses the at least one processing element is operable to enter the standby mode of operation when no data is received (see Figure 1, for example, no processing would occur when no data is inputted).

51. Consider claim 35, Kejriwal discloses each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

52. Consider claim 41, Clauberg discloses the architecture is implemented on a single integrated circuit (page 10, line 18, chip).

53. Consider claim 53, Marson discloses a processor comprising an architecture or system (page 2, first indented paragraph, the overall router is a processor as it processes data).

54. Consider claim 61, Marsan and Clauberg do not explicitly disclose processing is only performed by processing elements containing whole packets or packet portions carrying a header.

On the other hand, Kejriwal discloses processing is only performed by processing elements containing whole packets or packet portions carrying a header (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

Kejriwal's teaching of detecting whether a cell has packet header information, and only performing packet header operations if there is, enables the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kejriwal with the invention of Marsan

and Clauberg in order to enable the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

55. Consider claim 62, Marsan and Clauberg do not explicitly disclose processing is performed by multiple processing elements containing portions of a packet, in dependence on either data in the packet or information about the packet.

On the other hand, Kejriwal discloses processing is performed by multiple processing elements containing portions of a packet, in dependence on either data in the packet or information about the packet (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

Kejriwal's teaching of detecting whether a cell has packet header information, and only performing packet header operations if there is, enables the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kejriwal with the invention of Marsan and Clauberg in order to enable the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

56. Claims 22, 46 and 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marsan and Clauberg as applied to claim 1, 17, and 60 above, and further in view of ISSC95 (Evening Discussion Session).

57. Consider claims 22, 46, and 50, Marsan and Clauberg do not disclose that the architecture is implemented on a plurality of integrated circuits.

On the other hand, ISSC95 does disclose of architectures implemented on a plurality of integrated circuits (page 236, for example, multi-chip modules).

Multi-chip modules results in better yields, increased performance, and reduced cost, amongst other benefits (ISSC95, page 236, bottom two panelist statements, for example).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of ISSC95 with the invention of Marsan and Clauberg in order to gain better yields, increase performance, and reduce cost.

58. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marsan, Clauberg, and Kejriwal as applied to claim 12 above, and further in view of ISSC95 (Evening Discussion Session).

59. Consider claim 47, Marsan, Clauberg, and Kejriwal do not disclose that the architecture is implemented on a plurality of integrated circuits.

On the other hand, ISSC95 does disclose of architectures implemented on a plurality of integrated circuits (page 236, for example, multi-chip modules).

Multi-chip modules results in better yields, increased performance, and reduced cost, amongst other benefits (ISSC95, page 236, bottom two panelist statements, for example).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of ISSC95 with the invention of Marsan and Clauberg in order to gain better yields, increase performance, and reduce cost.

Response to Arguments

60. As referenced above, applicant's arguments made during an interview on 9/8/2008 regarding the pending final rejection made by a previous examiner were persuasive; thus, the current non-final rejection using significantly different prior art references is being issued.

Conclusion

61. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

f. Hirata (US 4755986) discloses of processing only a header of a packet on the basis of a data flow principle.

g. Marshall et al. (US 5420858) discloses of communication between a non-ATM communication medium to an ATM communication medium.

h. Follett (US 5440550) discloses of using parallel switching fabrics to switch slices of serial packets (subpackets) in a parallel manner.

i. Lincoln et al. (US 5768275) discloses of only processing a header which provides a faster response time.

j. Dai (US 5781549) discloses of packet segmentation and reassembly for cell-based switching using a plurality of packet processing units.

k. Ladwig et al. (US 6047304) discloses of an SIMD processor designed specifically for the task of network packet processing.

l. Merchant et al. (US 6081523) discloses of dividing packet data into segments and outputting using multiple physical layer devices to enable parallel transmissions to increase the effective data rate.

m. Mills et al. (US 6088355) discloses of pointer-based ATM segmentations and reassembly.

n. Laor et al. (US 6147996) and (US 6831923) discloses of a pipelined multiple issue packet switch.

o. Nakagoshi et al. (US 20010018732) discloses of splitting a packet, wherein each has a maximum permissible length.

p. Clauberg (US 6389018) discloses of on-the-fly processing of fixed length cells.

q. Kawarai et al. (US 20020122424) discloses of dividing a variable-length packet to parallel lines.

r. Sakamoto et al. (US 6836479) discloses of segmenting a variable length packet into fixed length cells and generating switching information based on the header information of the variable length packet.

s. Carr et al. (US 6963572) discloses of segmentation and reassembly of data packets in a communication switch.

t. Ganjali et al. (Input Queued Switches: Cell Switching vs. Packet Switching) discloses of cell-based systems which use fixed-size cells.

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 6:15 a.m. - 5:45 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183

/Keith Vicary/
Examiner, Art Unit 2183